

## CLAIMS

What is claimed is:

1           1.       An apparatus for setting an overflow flag based on a shift value and input data for one of  
2 a plurality of operations executed in a bit manipulation unit (BMU), the apparatus comprising:

3               a first logic circuit, for a first subset of the plurality of operations, setting a first overflow value  
4 based on the left shift value and the input data;

5               a second logic circuit, for a second subset of the plurality of operations, setting a second  
6 overflow value based on the right shift value and the input data; and

7               a selector providing either the first or the second overflow value as the overflow flag based on a  
8 signal identifying the one of the plurality of operations executed by the BMU.

1           2.       The invention as recited in claim 1, wherein the first logic circuit sets the first overflow  
2 value by:

3               1) comparing a number of redundant sign bits to a combination of the number of most significant  
4 bits (MSBs) of the input data and the shift value, and

5               2) setting the first overflow value based on the comparison, wherein  
6 the most significant bits correspond to bits at positions for a set of guard bits in the input data  
7 and at least one bit of the input data.

1           3.       The invention as recited in claim 2, wherein the first logic circuit comprises:

2               a saturator forming the combination; and

3               an exponent and compare module comparing the number of redundant sign bits based on the  
4 combination.

1           4.       The invention as recited in claim 1, wherein the second logic circuit sets the second  
2 overflow value by:

3               1) comparing the number of redundant sign bits to a combination of the most significant bits of  
4 the input data and the shift value, and

5               2) setting a second overflow value based on the comparison, wherein





3 circuit.

1           15.     A computer-readable medium having stored thereon a plurality of instructions, the  
2     plurality of instructions including instructions which, when executed by a processor, cause the processor  
3     to implement a method for setting a overflow flag based on a shift value and barrel-shifted input data for  
4     one of a plurality of operations executed in a bit manipulation unit (BMU), the method comprising the  
5     steps of:

6 (a) for a first subset of the plurality of operations, setting a first overflow value based on the left  
7 shift value and the input data;

8 (b) for a second subset of the plurality of operations, setting a second overflow value based on  
9 the right shift value and the input data; and

10 (c) selecting either the first or the second overflow value as the overflow flag based on a signal  
11 that identifies the one of the plurality of operations executed by the BMU.